Novel Intrinsic and Extrinsic Engineering for High-Performance High-Density Self-Aligned InGaAs MOSFETs: Precise Channel Thickness Control and Sub-40-nm Metal Contacts

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Abstract

We have fabricated self-aligned tight-pitch InGaAs Quantum-well MOSFETs (QW-MOSFETs) with scaled channel thickness (t_c) and metal contact length (L_c) by a novel fabrication process that features precise dimensional control. Impact of t_c scaling on transport, resistance and short channel effects (SCE) has been studied. A thick channel is favorable for transport, and a mobility of 8800 $cm^2/V{\cdot}s$ is obtained with t_c=11 nm at N_s=2.6x10^{12} cm^{-2}. Also, a record $g_{m,max}$ of 3.1 mS/μm and R_{on} of 190 Ω·μm are obtained in MOSFETs with t_c=9 nm and gate length L_g=80 nm. In contrast, a thin channel is beneficial for SCE control. In a device with t_c=4 nm and L_g=80 nm, S is 111 mV/dec at V_{ds}= 0.5 V. For the first time, working front-end device structures with 40 nm long contacts and gate-to-gate pitch of 150 nm are demonstrated. A new method to study the resistance properties of nanoscale contacts is proposed. We derive a specific contact resistivity between the Mo contact metal and the n^+ InGaAs cap of $\rho=(8\pm2)\text{x}10^{-9}$ Ω·cm^2. We also infer a metal-to-channel resistance of 70 Ω·μm for 40 nm long contacts.

Introduction

InGaAs is a promising channel candidate for CMOS applications [1,2]. However, the potential of InGaAs MOSFETs at realistic footprints has yet to be demonstrated. Advancing towards this goal requires precise lateral and vertical dimensional control in the intrinsic and extrinsic regions of the device. This work takes advantage of recent technological developments to study the impact of channel thickness and contact length on the performance of nanoscale InGaAs MOSFETs.

Recent prototype InGaAs QW-MOSFETs have attained great performance with $g_{m,max}\geq$2.7 mS/μm devices demonstrated by several groups [3-6]. In this work, we explore further performance gains by exploiting recently developed techniques to precisely thin-down the intrinsic portion of the channel of self-aligned InGaAs QW-MOSFETs. This has allowed us to carry out a systematic study of the impact of channel thickness on the electrical characteristics of transistors with minimum resistance parasitics. The devices obtained through this effort outperform previous demonstrations.

Realistic CMOS devices require scalable pitch and ohmic contact size. Very few MOSFET structures reported to date feature a tight contact pitch. The tightest devices still exhibit a rather large pitch length (L_p) such as L_p=500 nm in [8]. In this work, we fabricate self-aligned MOSFET test arrays with a sub-150 nm pitch size. This is a significant leap in an effort to meet the requirements of the ITRS 2013 roadmap for III-V CMOS logic [2]. In these test structures, we study the resistance properties of contacts down to 40 nm in length. In spite of the excellent results that have been obtained, this effort has revealed the need for further progress on nanoscale contacts.

Device fabrication

This work builds on our prior research on contact-first, self-aligned InGaAs QW-MOSFETs [6]. The device structure used in this research is sketched in Fig. 1a and a TEM of a L_g=40 nm transistor is shown in Fig. 1b.

The starting heterostructure (Fig. 2a) includes a 10 nm thick composite channel that consists (from top to bottom) of $In_{0.7}Ga_{0.3}As$ (3 nm), InAs (2 nm) and $In_{0.7}Ga_{0.3}As$ (5 nm). Above this there is a 3 nm InP barrier. Following a similar process as in [6], the heterostructure is etched with 1 nm precision in the intrinsic portion of the device through a combination of Cl_2-based RIE and digital etch (DE) (Fig. 2b). RIE stops a few nm above the cap. Then DE is used to finely thin down the channel to its final thickness [7]. As discussed in [7], achieving 1 nm channel thickness resolution does not require precise control of the final etching point of the RIE process.

Using this technique, we have fabricated devices in a process run that includes different splits with between 2 and 14 cycles of DE. The correlation between the number of DE cycles and the resulting t_c is shown in Fig. 2a. Here t_c denotes the total thickness of the channel heterostructure which includes all layers between the InAlAs buffer and the gate oxide including the InP barrier if present. Thus, a buried-channel device is obtained when t_c>10 nm, otherwise a surface-channel device results. Our process yielded identical transistors except for the value of t_c which varied from 12 nm down to 3 nm. TEMs of final devices for two etch depths are shown in Fig. 2c for devices with t_c of 4 nm and 8 nm, confirming our calibrations.

The rest of the fabrication process is similar to that of [6]. The gate oxide is 2.5 nm HfO_2 deposited by ALD. Device L_g spans from 40 nm to 5 μm. The length of the access region measured from the edge of the gate to the edge of the contact between the ohmic metal and the n^+ cap is L_{access}=15 nm (Fig. 1). The contacts have a length L_c=10 μm.

To examine the lateral scalability of our process and to study the resistance of nanoscale contacts, we simultaneously fabricated MOSFET arrays on the same chip. These consist of multiple series-connected transistor cells with scaled gates and contacts. The devices have L_g between 30-130 nm, L_c between 40-800 nm and L_{access}=15 nm. More details are given below.

High-Performance InGaAs MOSFETs

Our results show that channel thickness scaling exerts a very significant influence on the MOSFET electrical characteristics. From the ON-current point of view, t_c=9 nm is most favorable. A L_g= 80 nm device with t_c=9 nm exhibits a peak transconductance of $g_{m,max}$=3.1 mS/μm at V_{ds}=0.5 V (Fig. 3). We believe this is the highest g_m III-V transistor ever made exceeding the most advanced InGaAs MOSFETs and HEMTs [3-6, 10]. The output characteristics of this device, shown in Fig. 4, indicate an unprecedented R_{on} of 190 Ω.μm. A minimum subthreshold swing (S_{min}) of 159 mV/dec at V_{ds}=0.5 V and DIBL=310 mV/V are also obtained in the same device (Fig. 5a). Benchmarking of this device against recently published InGaAs MOSFETs (Fig. 6) indicates an outstanding balance between transport and subthreshold characteristics.

Thin channel devices exhibit superior subthreshold behavior as seen in Fig. 5b for a t_c=4 nm transistor where S=111 mV/dec at V_{ds}=0.5 V and DIBL=126 mV/V. This comes at the expense of g_m and ON-current that are both seriously compromised.

In a systematic study of the impact of t_c on key figures of merit, Fig. 7 shows $g_{m,max}$ *vs.* t_c for devices with L_g from 80 nm to 5 μm. $g_{m,max}$ always peaks at t_c=9 nm. For $t_c \geq 10$ nm, the gate dielectric sits on the InP barrier (buried channel). Thus capacitive coupling to the channel is reduced. For $t_c \leq 8$ nm, the transport and resistance characteristics degrade prominently. This is also shown in Fig. 8 that graphs R_{sd} ($=R_s+R_d$) *vs.* t_c. R_{sd} is obtained from measurements of R_{on} *vs.* L_g at $V_{gs}-V_t$=0.5 V. The rise of R_{sd} for very thin t_c highlights the role of the spreading resistance associated with the link region at the gate edge of the channel.

In contrast with transport figures of merit, SCE control is improved by reducing t_c, as shown in Figs. 9, 10 and 11. Thinner t_c leads to improved S, DIBL and $V_{t,sat}$ *vs.* L_g characteristics. For $t_c \leq 4$ nm, the improvements tend to saturate.

To further understand charge control and transport in these devices, we have carried-out split-C-V measurements on long-channel MOSFETs (L_g=5 μm) at 1 MHz (Fig. 12). The ON-state capacitance increases monotonically as the channel is thinned down. Two factors contribute to this. First, as t_c is reduced, the centroid of charge moves closer to the gate. Second, for thin enough t_c, the InAs core is eventually removed and the electron effective mass increases. This yields an improved saturation behavior of the C-V characteristics for t_c=3 nm. In all cases, very low gate leakage current flows, as shown in the inset of Fig. 12 for t_c=9 nm.

The effective mobility (μ_{eff}) was extracted by split-C-V method on the L_g=5 μm devices after correcting for R_{sd} (Fig. 13). We find significant mobility degradation as the channel is thinned down due to increased interface scattering and the eventual extinction of the InAs core. This is consistent with [11]. In an MBE calibration heterostructure (same channel configuration but with a thin cap) we obtained a Hall mobility of $\mu_{H,max}$= 11,000 $cm^2/V{\cdot}s$ at $N_s=2.6{\times}10^{12}$ cm^{-2}. This confirms the excellent intrinsic transport properties of our as-grown material. For t_c=11 nm, μ_{eff} at $N_s=2.6{\times}10^{12}$ cm^{-2} is 8800 $cm^2/V{\cdot}s$, about 80% of $\mu_{H,max}$. To the authors' knowledge, this is the highest μ_{eff} [1,12] in an InGaAs/InAs channel MOSFET. The degradation of μ_{eff} with respective to $\mu_{H,max}$ could be due to interface roughness scattering that is exacerbated by the 1 nm InP barrier (*vs.* 3 nm in the calibration heterostructure) that is present in the t_c =11 nm device.

High-Density InGaAs MOSFET Arrays

To study the characteristics of InGaAs MOSFETs with scaled pitch, we have fabricated MOSFET arrays and gate-less arrays as sketched in Figs. 14 a and b. The gate-less array has a similar structure as the MOSFET array except that the n^+ cap is not recessed and a gate is not fabricated. In the MOSFETs array, one cell (one pitch size) consists of one gate length, one contact length and two access lengths. Arrays with different numbers of cells and various gate and contact dimensions have been fabricated. These structures allow us to extract all the relevant resistance components of a tight-pitch MOSFET.

We have fabricated arrays with 1 to 4 transistor cells, as illustrated in Fig. 14. Pitch sizes varied between L_p=100 nm and ~1 μm. The channel thickness was 9 nm. Cross sectional TEM views of two MOSFET arrays are shown in Fig. 15. Fig. 15a shows a 1-cell array with L_p=200 nm, L_c=40 nm, and L_g=130 nm. Fig. 15b shows a 2-cell array with L_p=150 nm, L_c=80 nm, and L_g=40 nm. Gates in each cell are connected together and biased at V_g, while the inner contacts are floating. The two ends of the arrays are biased at V_d and V_s respectively. In all these arrays, we measure the total resistance *vs.* number of cells. In addition, for the MOSFETs array the gate is biased at $V_{gs}-V_t \gg V_{ds}$. The unit-cell resistance (R_{cell}) is determined from the slope of a graph of total resistance *vs.* number of cells (Fig. 16). Figs. 17 and 18 show unit-cell resistance *vs.* L_c for both types of arrays.

A resistor network model is developed to analyze these results. Cross-section schematics and equivalent circuit models of both array types are shown in Fig. 19. For small enough V_{ds}, the channel in both arrays can be modeled as a simple resistor. In the MOSFET array, the contact can be modeled by a 2D resistor network composed of three coupled lateral conducting layers (Fig. 19b). The two vertical resistive couplings are characterized by two unknown contact resistivities, ρ_{12} and ρ_{23}. In the gate-less array, a single contact resistivity ρ_{12} couples two lateral conducting layers. ρ_{12} and ρ_{23} can then be extracted by fitting the model to the experimental results of Figs. 17 and 18 after the rest of the model parameters are obtained from independent TLM or Hall measurements (Table I).

We obtain $\rho_{12}=(8\pm2){\times}10^{-9}$ $\Omega{\cdot}cm^2$ for the contact resistivity between the Mo contact and the n^+ cap from the gate-less array (Fig. 17), and $\rho_{23}=(2\pm0.8){\times}10^{-8}$ $\Omega{\cdot}cm^2$ for the contact resistivity between the n^+ cap and the channel from the MOSFET array (Fig. 18). The value of ρ_{12} is consistent with independent measurements carried out in nano-TLMs [13] and other Mo/InGaAs contact experiments [14] and is much lower than other metal to InGaAs contact technologies [9].

We use these extracted values to estimate the vertical contact resistance, R_c, of scaled MOSFETs fabricated by our technology. R_c here refers to the resistance from the metal contact to the edge of the access region, or points C and A in Fig. 14b. The result for different values of L_c is plotted in Fig. 20. We infer a metal-to-channel resistance of 70 Ω·μm for 40 nm long contacts. These are encouraging results but more research is required to attain the required R_c in nanometer-scale contacts.

Conclusions

We have studied the role of body thickness on the electrical characteristics of self-aligned InGaAs QW-MOSFETs. In an optimized design with thick channel thickness, we have obtained a record $g_{m,max}$ of 3.1 mS/μm and a mobility of 8800 $cm^2/V{\cdot}s$ at $N_s=2.6{\times}10^{12}$ cm^{-2}. We have also fabricated front-end MOSFET test structures with 40 nm contact size and scaled contact pitch. A model is developed to study the characteristics of nano-scale contacts. A low contact resistivity of $\rho=(8\pm2){\times}10^{-9}$ $\Omega{\cdot}cm^2$ between Mo and n^+ InGaAs is derived from this study.

Acknowledgements

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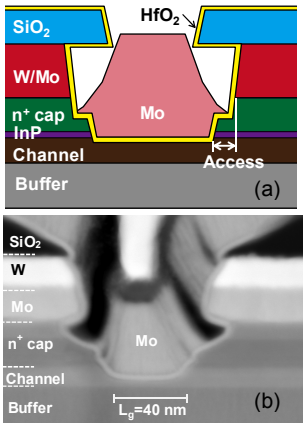

Fig. 1 (a) InGaAs MOSFET cross section schematic, and **(b)** TEM image of a complete device with L_g=40 nm and 2.5 nm HfO_2 gate dielectric.

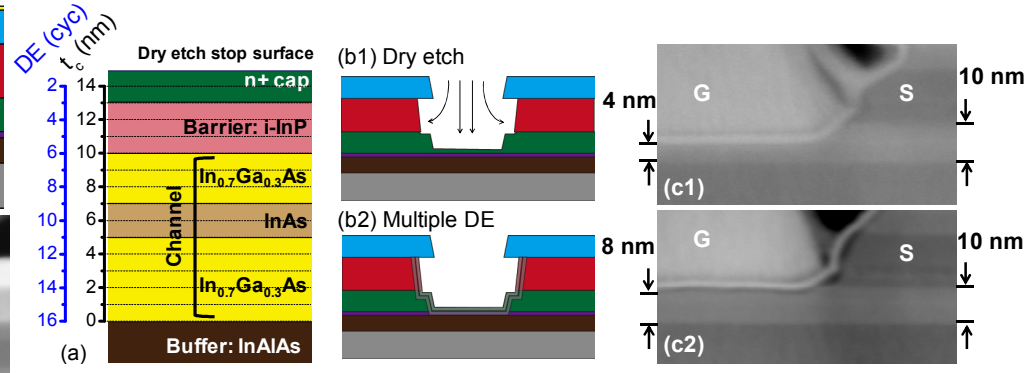

Fig. 2 (a) Correlation between number of DE cycles and final channel thickness, t_c, in the grown heterostructure. **(b)** Precise etching process of the intrinsic region of the device is performed by RIE (b1) and DE (b2). The RIE stops a few nm above the channel surface. The final channel thickness is controlled by DE with 1 nm precision. **(c)** TEM images of finished devices with two t_c thicknesses. In the extrinsic portion, the as-grown total channel thickness is 10 nm. In the intrinsic portion, the resultant t_c are 4 nm (c1) and 8 nm (c2).

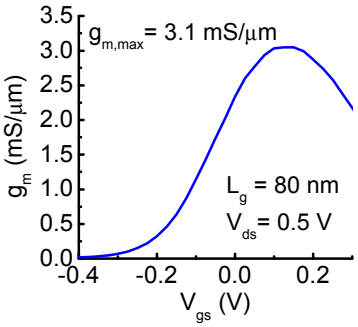

Fig. 3 Transconductance of InGaAs MOSFET with t_c =9 nm and L_g=80 nm.

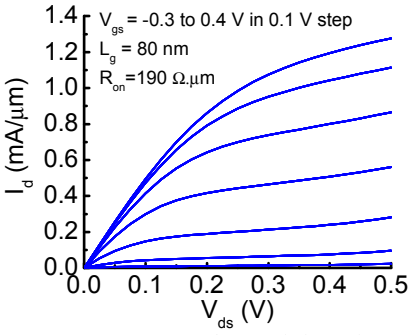

Fig. 4 Output characteristics of device of Fig. 3.

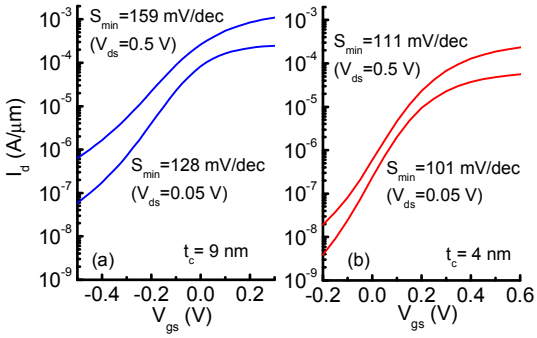

Fig. 5 Subthreshold characteristics of two L_g= 80 nm MOSFET with **(a)** t_c=9 nm (same device of Fig. 3, optimized for ON-current) and **(b)** t_c=4 nm (optimized for SCE).

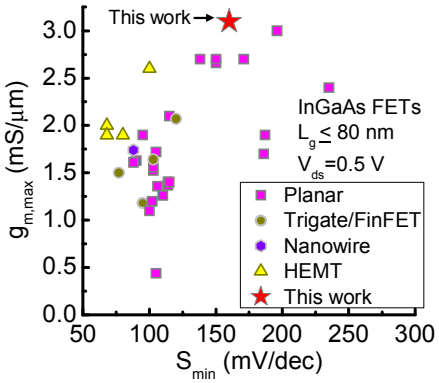

Fig. 6 Benchmarking of $g_{m,max}$ *vs.* S at 0.5 V for III-V FETs with L_g≤80 nm showing record device obtained in this work.

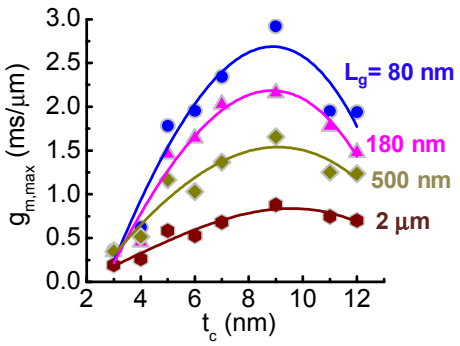

Fig. 7 Peak transconductance *vs.* t_c for transistors with L_g from 80 nm to 2 μm.

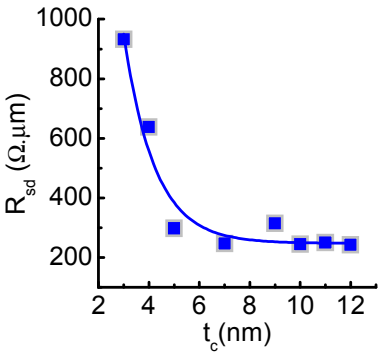

Fig. 8 R_{sd} *vs.* t_c. R_{sd} is extracted from measurements of R_{on} *vs* L_g.

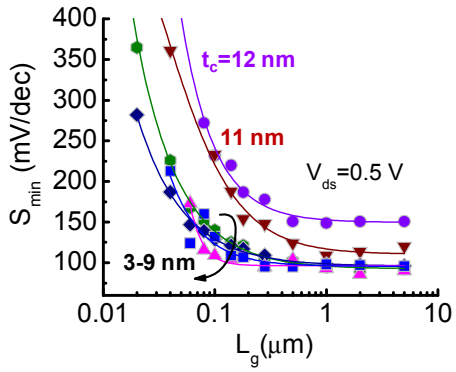

Fig. 9 Subthreshold swing at V_{ds}=0.5 V *vs.* L_g for MOSFETs with t_c from 3 nm to 12 nm.

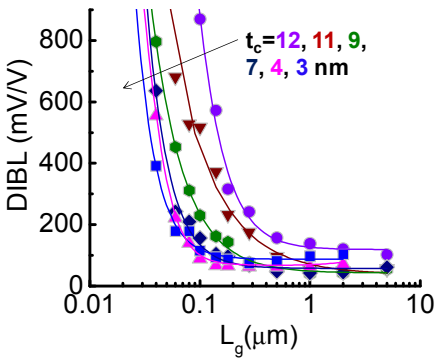

Fig. 10 DIBL *vs.* L_g for MOSFETs with t_c from 3 nm to 12 nm.

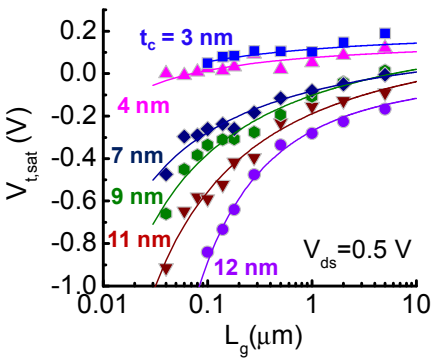

Fig. 11 $V_{t,sat}$ *vs.* L_g for MOSFETs with different t_c.

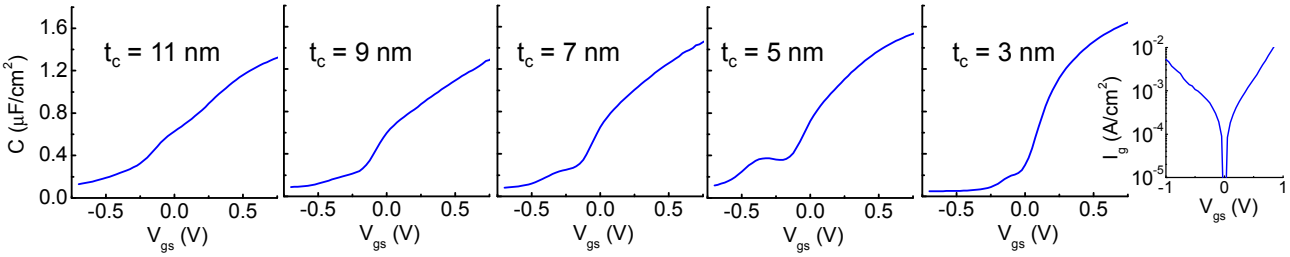

Fig. 12 C-V characteristics measured on devices with L_g=5 μm for different t_c at 1 MHz. Inset gives the typical gate leakage current density, in this case for t_c=9 nm.

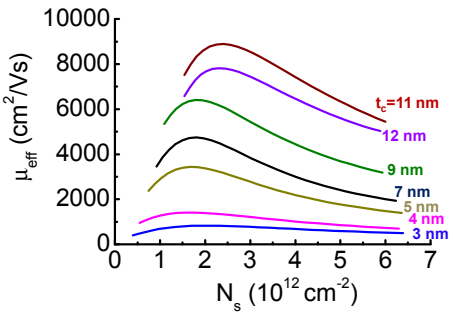

Fig. 13 Mobility *vs.* sheet carrier density for t_c from 12 nm to 3 nm.

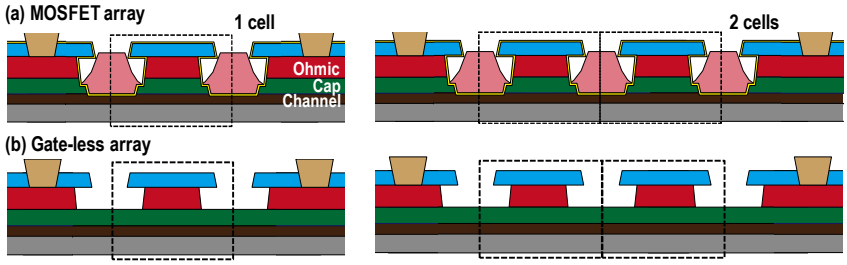

Fig. 14 Cross-section schematic of: **(a)** tight-pitch MOSFET arrays; (b) gate-less arrays. Schematics show examples with 1 cell (left) and 2 cells (right).

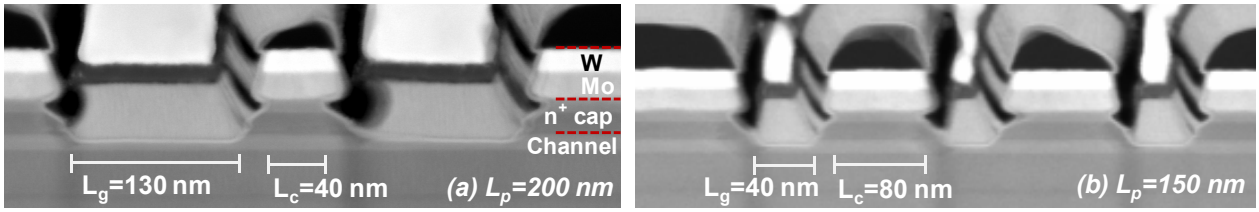

Fig. 15 TEM of tight-pitch MOSFET array with different pitch size (L_p), contact length (L_c) and gate length (L_g): **(a)** One-cell array with L_p=200 nm, L_c=40 nm, and L_g=130 nm; **(b)** Two-cell array with L_p=150 nm, L_c=80 nm, and L_g=40 nm.

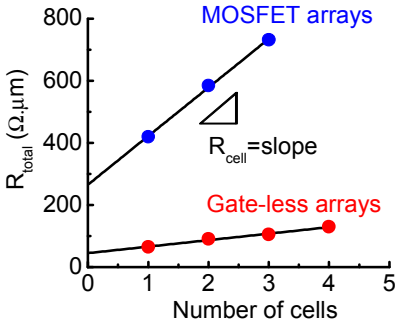

Fig. 16 Extraction of unit-cell resistance (R_{cell}) from slope of total resistance *vs.* number of cells in gate-less arrays and MOSFET arrays.

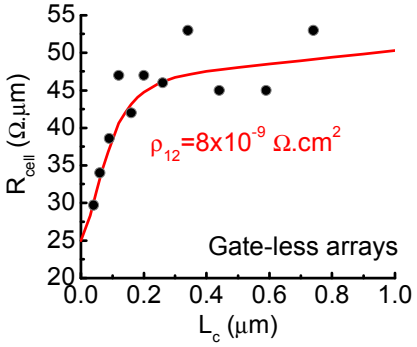

Fig. 17 Unit-cell resistance *vs.* contact length in gate-less arrays (Fig. 14b). ρ_{12} is extracted.

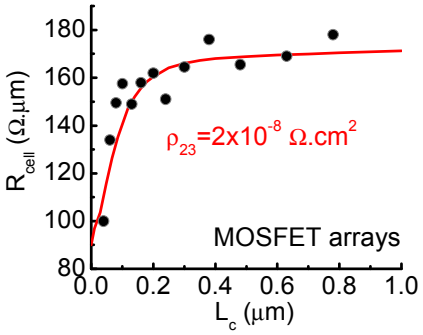

Fig. 18 Unit-cell resistance *vs.* contact length in MOSFET arrays (Fig. 14a). ρ_{23} is extracted.

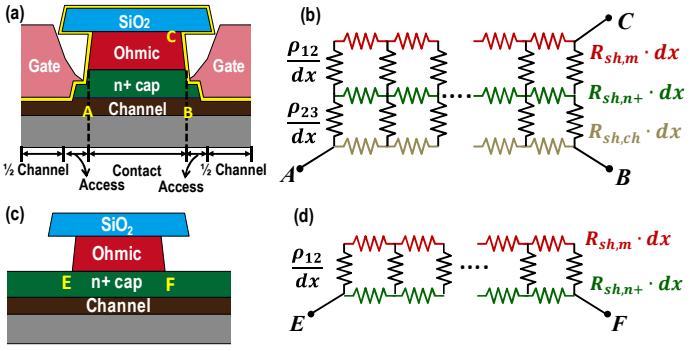

Fig. 19 (a) Cross-section schematic of unit cell of MOSFET array and **(b)** equivalent circuit model. **(c)** Cross-sectional schematic of unit cell of gate-less array and **(d)** equivalent circuit model.

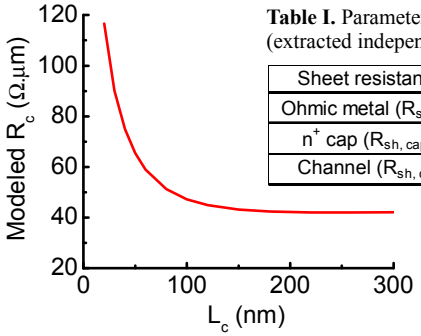

Fig. 20 Modeled vertical contact resistance *vs.* contact length of InGaAs QW-MOSFETs based on the extracted parameters that characterize our contact system. This is the estimated resistance between nodes A and C with B floating in Fig. 19a.

Table I. Parameter used in modeling (extracted independently).

Sheet resistance	Value (Ω/□)
Ohmic metal ($R_{sh,m}$)	4.6
n^+ cap ($R_{sh,cap}$)	170
Channel ($R_{sh,ch}$)	700